UNIFIED LEARNING PLATFORM FOR EMBEDDED ENGINEERING
FP7-ICT-2011-8 / 317882

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BALCON Belgrade 2013
MOTIVATION: Overcoming high barrier in engineering studies of embedded systems

- variety of structure (processor, communication, sensor)
- variety of applications (automation, automotive, consumer)

GOAL: Unified learning platform for studies of embedded systems

- modular and scalable
- equipped with education-oriented tools
- accompanied with set of exercises in open-source library
PROJECT DATA:

Acronym: E2LP
Identifier: FP7-ICT-2011-8 / 317882 (CP)
Budget: 2.095.884 EUR
Start: 01.09.2012
Duration: 36 months
Consortium: 4 universities, 3 research, 2 SME
CONSORTIUM:

1. Faculty of technical sciences, Univ. Novi Sad, Serbia (coordinator)
2. RD Institute Rudjer Boskovic, Zagreb, Croatia
3. Faculty of engineering, Univ. Freiburg, Germany
4. Commissariat a l’energie atomique et aux energies alternatives, Paris, France
5. RD Institute for automation and measurements, Warsaw, Poland
6. Creativitic Innova SL, La Rioja, Spain (SME)
7. RD Institute RT-RK, computer based systems Novi Sad, Serbia (SME)
8. Faculty of electrical engineering and computing, Univ. Zagreb, Croatia
9. Ben Gurion university of Negev, Israel
E2LP kickoff meeting: Paris 01.10.2012
FIVE TOUCHABLE OUTPUTS:

1. E2LP platform (mother and extension boards)

2. Basic set of exercises

3. AR (augmented reality) interface

4. Remote lab (Internet portal)

5. Evaluation methodology with tools
E2LP PLATFORM:

1. **Basic module (mother board)**
   - host controller (ARM)
   - interfaces (USB, HDMI, LAN, …)
   - Interconnection setup (FPGA)

2. **Extension modules (daughter boards)**
   - Armada based (Marvel)
     . Multimedia
     . Wireless
     . System SW (Linux / Android)
   - ARM based
     . Microcontrollers
     . Sensor Networks
# BASIC SET OF EXERCISES:

<table>
<thead>
<tr>
<th>Sem.</th>
<th>Course</th>
<th>Professor</th>
<th>Assistant</th>
<th>Labs</th>
<th>Total</th>
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<tbody>
<tr>
<td>3</td>
<td>LPRS 1</td>
<td>Nikola Teslić Nebojša Pjevalica</td>
<td>Ivan Kaštelan</td>
<td>1. Digital Logic Circuits &amp; VHDL Gate-Level Design</td>
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<td>2. Combinational Circuits</td>
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<td>3. Problem Set: Multiplexing Adders</td>
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<td>4. Sequential Circuits</td>
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<td>5. Problem Set: Stopwatch</td>
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<td>6. Finite State Machines</td>
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<td>7. Problem Set: Car Turn Signals</td>
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<td>8. Complex Digital Systems</td>
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<td>9. Problem Set: LCD Banner</td>
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<td>10. Computation Structures</td>
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<td>11. Problem Set: Fixed Computation Structure</td>
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<td>5</td>
<td>ORM 1</td>
<td>Ilija Basičević</td>
<td>Stanislav Očovaj</td>
<td>1. ISO OSI Layer 1</td>
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<td>2. ISO OSI Layer 2</td>
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<td>3. User Datagram Protocol (UDP)</td>
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<td>4. Transmission Control Protocol (TCP)</td>
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<td>5. File Transfer Protocol (FTP)</td>
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<td>6. HyperText Transfer Protocol (HTTP)</td>
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</table>
| 5    | DSP 1  | Miodrag Temerinac  | Željko Lukač    | 1. Digital Filters - FIR Filter  
2. Digital Filters - IIR Filter                                        | 2     |
|      |        |                    |                 | 1. Multitasking - Critical section                                   |       |
|      |        |                    |                 | 2. Multitasking – Producer-consumer                                   |       |
|      |        |                    |                 | 3. Multitasking – Timers                                              |       |
|      |        |                    |                 | 4. Linux drivers – GPIO control without interrupts                    |       |
|      |        |                    |                 | 5. Linux drivers – SIO/PIO and time control and with interrupts       |       |
| 5    | SPPRV 2| Miroslav Popović   | Miodrag Đukić,  | 1. Audio postprocessing                                               | 5     |
|      |        |                    | Vladimir Marinković| 2. Noise reduction in still image                                      |       |
|      |        |                    |                 | 3. Image interpolation                                                |       |
| 6    | DSP 2  | Miodrag Temerinac  | Željko Lukač    | 1. Analysis of Ethernet Frame Structure and Data Flow                 | 3     |
|      |        |                    |                 | 2. Analysis of IP and TCP/IP Packet Structure and Data Flow           |       |
|      |        |                    |                 | 3. Implementation of Server-Client Architecture                       |       |
| 6    | ORM 2  | Dragan Samardžija | Miloš Pilipović  | 4. Analysis of WiFi Frame Structure and Data Flow                     | 7     |
|      |        |                    |                 | 5. Introduction to 802.15.4/ZigBee                                   |       |
|      |        |                    |                 | 6. Implementation of Multi-hop 802.15.4 System                        |       |
|      |        |                    |                 | 7. Implementation of 802.15.4/Ethernet Gateway                       |       |
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| 6    | LPRS 2 | Branislav Atlagić | Dušan Majstorović  | 1. Clock management techniques  
2. VGA interface  
3. Simple RISC processor  
4. Xilinx Platform Studio (XPS) introduction  
5. XPS video adapter  
6. XPS advanced  
7. XPS project | 7     |
| 6    | PNRS 1 | Istvan Papp       | Milan Bjelica      | 1. Introduction to Android application development for embedded devices  
2. Android user interface development  
3. Working with multimedia in Android  
4. Creating custom widgets in Android  
5. Networking in Android  
6. Internet in Android  
7. Working with Android services  
8. Permanent data storage in Android  
9. Home Screen Widgets in Android  
10. Native Android programming  
11. OpenGL programming showcase in native code  
12. Student project | 12    |
AUGMENTED REALITY INTERFACE IN EDUCATION

- information merge of data and hardware
- associative understanding for students
- easy to extend
REMOTE LAB

- open source library of exercises
- background behavior analysis and adjustment
- assistance for students
- evaluation and guidance in education process
EVALUATION TOOLS

Students responses

Teachers responses
TIMELINE:

1st year
- Requirements and specifications
- First version of the E2LP platform
- Basic set of exercises

2nd year
- E2LP verification & improvement at universities in consortium
- AR interface
- Remote lab (IP platform with open source exercise sets)

3rd year
- Evaluation methodology with tools
- Propagation to other EU universities
Thank you.  Questions?

www.e2lp.com
miodrag.temerinac@rt-rk.com